

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6. (Cancelled)

7. (currently amended) A serial communication device, comprising:

a central processing unit ~~for executing~~ to execute a program;

a serial communication interface coupled to receive data from ~~an outside of the~~ serial communication device and ~~providing to provide a~~ transfer request signal and a timeout interrupt signal, ~~wherein the~~ timeout interrupt signal ~~is~~ being provided to the central processing unit when the data from ~~the outside of the~~ serial communication device is not received by the serial communication interface stopped for a certain predetermined time;

a RAM including:

a buffer area ~~for storing to store~~ the data, and  
a work area for the program; and

a direct memory access controller coupled to receive the transfer request signal and ~~transferring to transfer~~ the

data from the serial communication interface to the buffer area, the direct memory access controller ~~being having~~ set therein a first number as a number of ~~transfer-transfers,~~ ~~which is the first number being larger-greater~~ than a second number corresponding to a number of data received at a time by the serial communication interface,

wherein the direct memory access controller provides a data transfer end interrupt signal to the central processing unit when a transfer number of data received by the serial communication interface reaches the first number, and

wherein ~~the any~~ data stored in the buffer area is transferred to the work area by the direct memory access controller when the central processing unit ~~receive-receives~~ the data transfer end interrupt signal or the timeout interrupt signal.

8. (currently amended) A serial communication device according to claim 7,

wherein the serial communication interface includes a first-in first-out memory in which to store the data from ~~the outside of the~~ serial communication device, ~~is stored,~~ and

wherein the transfer request signal is provided to the direct memory access controller when a number of data

received in the first-in first-out memory ~~is exceeded~~  
exceeds a number of data received trigger set in the serial  
communication interface.

9. (currently amended) A serial communication device  
according to claim 7,

wherein the direct memory access controller is started  
up before the serial communication interface receives the  
data from outside the serial communication device, and

wherein the first number is set in the direct memory  
access controller before the serial communication interface  
receives the data.

10. (currently amended) A serial communication device  
according to claim 9, wherein the serial communication  
interface further includes a means for stopping the  
generation of ~~the next data receive~~ to be received by the  
serial communication interface from outside the serial  
communication device after the timeout interrupt signal has  
been ~~enee~~ generated.

11. (currently amended) A serial communication device  
comprising:

a central processing unit ~~for executing to execute~~ a program;

a serial communication interface coupled to receive data from ~~an outside of~~ the serial communication device and ~~providing to provide~~ a transfer request signal, the serial communication interface including a timeout interrupt signal generation section ~~for providing to provide~~ a timeout interrupt signal to the central processing unit ~~according to~~ based on a timeout setting value for a period until the timeout interrupt signal is generated;

a memory including:

a buffer area ~~for storing to store~~ the data, and  
a work area for the program; and

a direct memory access controller coupled to receive the transfer request signal and ~~transferring to transfer~~ the data from the serial communication interface to the buffer area, the direct memory access controller ~~being having set~~ therein a first number as a number of transfers, the first number being which is larger greater than a second number ~~as corresponding to~~ a number of data received at a time by the serial communication interface,

wherein the direct memory access controller provides a data transfer end interrupt signal to the central processing unit when a number of data transferred from the serial

communication interface to the buffer area by the direct memory access controller reaches the first number, and

wherein ~~the~~any data stored in the buffer area is transferred to the work area by the direct memory access controller when the central processing unit ~~receive~~receives one of the data transfer end interrupt signal and the timeout interrupt signal.

12. (currently amended) A serial communication device according to claim 11, wherein the timeout interrupt signal generation section includes:

a receive determination section coupled to receive the data from outside ~~of the~~ serial communication device and ~~providing to provide~~ a count start trigger when the data is received;

a counter coupled to receive the count start trigger and ~~providing to provide~~ a count value; and

an overflow determination section coupled to receive the count value and the timeout setting value and ~~providing to provide~~ the timeout interrupt signal when the count value is ~~exceeded~~exceeds the timeout setting value.

13. (currently amended) A serial communication device according to claim 12, wherein the timeout interrupt signal

generation section further includes a register ~~for storing~~  
to store the timeout setting value.

14. (currently amended) A serial communication device according to claim 13, wherein the serial communication interface is configured to further has function for stopping ~~the stop~~ generation of the timeout interrupt signal until the next data ~~receive~~ received by the serial communication interface, after the timeout interrupt signal has been ~~once~~ provided.

15. (currently amended) A serial communication device according to claim 11,

wherein the serial communication interface includes a first-in first-out memory ~~in which to store~~ the data from ~~the outside of the serial communication device,~~ is stored, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory ~~exceeded~~ exceeds a number of data received trigger set in the serial communication interface.

16. (currently amended) A serial communication device according to claim 11,

wherein the direct memory access controller is started up before the serial communication interface receives the data from outside the serial communication device, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

17. (currently amended) A serial communication device comprising:

a central processing unit ~~for executing~~ to execute a program;

a serial communication interface coupled to receive data from ~~an outside of~~ the serial communication device and ~~providing to~~ provide a transfer request signal, the serial communication interface including a timeout interrupt signal generation section ~~for providing to~~ provide a timeout interrupt signal to the central processing unit ~~according to~~ based on a timeout value for a time period until the timeout interrupt signal is generated;

a memory including:

a first buffer area,

a second buffer area, and

a work area for the program; and

a direct memory access controller having a continuous transfer function and coupled to receive the transfer request signal and ~~transferring to transfer~~ the data from the serial communication interface to one of the first buffer area and the second buffer area, the direct memory access controller providing a data transfer end interrupt signal to the central processing unit and changing a destination of a data transfer to the other of the first buffer area and the second buffer area, ~~is full with the data,~~

wherein ~~the any~~ data stored in the one of the first buffer area and the second buffer area is transferred to the work area by the direct memory access controller when the central processing unit ~~receive~~ receives one of the data transfer end interrupt signal and the timeout interrupt signal.

18. (currently amended) A serial communication device according to claim 17,

wherein the serial communication interface includes a first-in first-out memory ~~where to store~~ the data from the outside ~~of the~~ serial communication device, ~~is stored,~~ and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory ~~exceeded~~ exceeds a number of data received trigger set in the serial communication interface.

19. (currently amended) A serial communication device according to claim 17,

wherein the direct memory access controller is started up before the serial communication interface receives the data from outside the serial communication device, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

20. (currently amended) A serial communication device according to claim 17,

wherein the timeout interrupt signal generation section includes:

a receive determination section coupled to receive the data from ~~the outside of the~~ serial communication device and ~~providing to provide~~ a count start trigger when determining a reception of the data by the serial communication interface;

a counter to provide a count value, the counter being  
responsive to the count start trigger ~~and starting its count~~  
up operation; ~~and providing a count value; and~~

an overflow determination section ~~comparing to compare~~  
the count value with the timeout setting value and ~~providing~~  
to provide the timeout interrupt signal according to based  
on a result of the comparison being that the count value is  
has exceeded the timeout setting value.

21. (currently amended) A serial communication device  
according to claim 20, wherein the timeout interrupt signal  
generation section further includes a register ~~for storing~~  
to store the timeout setting value.

22. (currently amended) A serial communication device  
according to claim 20,

wherein the direct memory access controller has a first  
channel and a second channel,

wherein one of the first channel and the second channel  
is used for ~~a data transfer from the serial communication~~  
unit to ~~the one of the first buffer area and the second~~  
buffer area, while the other of the first channel and the  
second channel is used for a data transfer from the other of

the first buffer area and the second buffer area to the work area.

23. (currently amended) A serial communication device according to claim 17, wherein the serial communication interface ~~further includes a function~~ is configured to stop the generation of the timeout interrupt signal until the serial communication interface receives next data, after the timeout interrupt signal is provided.